REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 4-7, 10-13 and 16-28 are presently active in this case, Claims 1, 7, and 13 having been amended by the present Amendment.

In the outstanding Official Action Claims 1, 4-6, 13, 22, 26 and 28 were rejected under 35 USC 103(a) as being unpatentable over Nowak et al., (U.S. Patent 6,191,451); Claims 7, 10-12 and 27 were rejected under 35 USC 103(a) as being unpatentable over Nowak et al as applied to Claim 1 above, and further in view of Stolmeijer et al (U.S. Patent 5,742,090); and Claims 16-19 were allowed.

Applicants acknowledge with appreciation the allowance of Claims 16-19.

In light of the several grounds for rejection, Claim 1 has been amended to clarify the claimed subject matter. To that end, amended claim 1 recites a semiconductor device comprising a low resistance area which has a resistive value lower than that of the well area, which is in contact with element isolation areas, and which is not in contact with a depletion layer of junction portions between semiconductor layers and the well area. The low resistance area is in contact with the base portion of the well area, and connects the first and second areas. Since resistive values of areas below the element isolation areas can be lowered, the well resistance can be kept low even when the element isolation areas are enlarged. As a result, thermal noise can be prevented.

Similarly, Claim 7 has been amended to recite a semiconductor device comprising a first low resistance area which has a resistive value lower than that of the first well area, which is in contact with element isolation areas, and which is not in contact with a depletion layer of a junction portion between source/drain regions of the MOS transistor and the first

well area. The first low resistance areas are in contact with the base portion of the first well area, and connect first and second areas. Since the first semiconductor layer is formed in the second area, and the MOS transistor formed in the first area are connected by the first low resistance area, parasitic resistance of the first well area can be reduced. Accordingly, potential supplied to the first semiconductor layer can be supplied to the well area without any loss, thereby configuring a high-gain amplifier.

In addition, claim 13 has been amended to recite a semiconductor device comprising a first low resistance area which has a resistive value lower than that of the first well area, which is in contact with element isolation areas, and which is not in contact with a depletion layer of a junction portion of a bipolar transistor. The first low resistance area is in contact with the base portion of the first well area, and connects the first and second areas. Since the third electrode is formed in the second area, and the first and second electrodes formed on the first area are connected by the first low resistance area, parasitic resistance of the first well area can be reduced. Accordingly, power loss of the bipolar transistor can be prevented, thereby configuring a high-gain amplifier.

Nowak et al. discloses an SOI semiconductor device having an improved decoupling capacitance. To that end, the Nowak et al. of FIG. 2 includes N-wells 132, 134 formed in a bulk area 130, and isolation layers 20 formed in the bulk area 130 and the N-wells 132, 134. Further, N+ regions 136, 144 and a P+ region 138 are formed in the N-wells 132, 134 which are isolated by isolation layers 20.

The outstanding Office Action points out that the P+ implant 140 of Nowak et al. is a low resistance area. However, the P+ implant 140 does not contact the isolation layers 20 as the acknowledged in the outstanding Office Action. Further, however, the P+ implant 140 is not in contact with the N-wells 132, 134. The P+ implant 140 does not connect the areas

including the N+ regions 136, 144 and the P+ regions 138, 142, isolated by isolation layers. Moreover, the P-type dopant 140 is an optional layer which can be used for added capacitance, as described at column 2, lines 60-62 and at column 2, line 68 to column 3, line 1 of Nowak et al. Therefore, the P-type dopant 140 of Nowak et al. does not suggest the advantages of the present invention, i.e., (i) preventing thermal noise (claim1); (ii) improving the gain of an amplifier (claim 7); and (iii) preventing power loss of a bipolar transistor, thereby improving the gain of an amplifier (claim 13). In addition, the P-type dopant 140 is an optional layer which can be used for added capacitance, as described at column 2, lines 60-62 and at column 2, line 68 to column 3, line 1 of Nowak et al.

As described above, the Nowak et al. device differs in structure, function and result from the claimed invention recited in Claims 1, 7 and 13. It is therefore respectfully submitted that Claims 1, 7 and 13 are patentably distinguishing over Nowak et al.. Since the deficiencies of Nowak et al.. are not remedied by Stolmeijer et al, it is respectfully submitted that the outstanding grounds for rejection have been overcome.

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed to be outstanding, and the present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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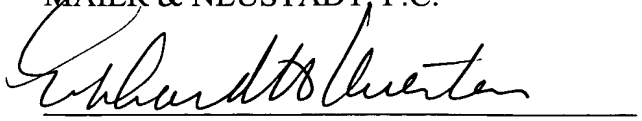

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